

## **ABSTRACT OF THE DISCLOSURE**

To reduce cost of defect redundancy and trimming in a semiconductor integrated circuit having multiple layer wirings and copper wirings, an address for salvaging a defect of a memory cell array in a semiconductor is stored by using a  
5 nonvolatile memory element constituting a floating electrode by a first layer of polysilicon, or the nonvolatile memory element is programmed in testing the semiconductor integrated circuit. As a result, a special process is not needed in forming the nonvolatile memory element. In other words, the nonvolatile memory element can be formed in a process of forming a CMOS device and an  
10 apparatus of a laser beam for programming is not needed since the programming is carried out in testing. Thus, the time necessary for programming can be shortened, and, therefore, testing costs can be reduced.